AN3472

Implementing Auxiliary Power in PoE

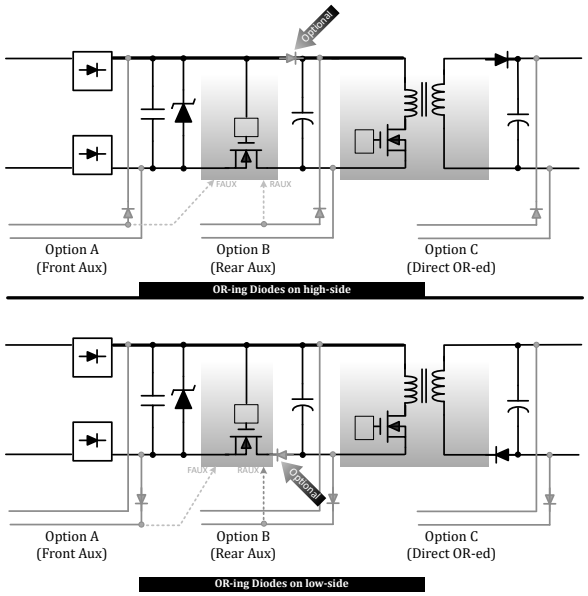
Introduction

Many PoE applications employ auxiliary power sources, typically an AC-powered “wall wart” or a solar panel, connected to the Powered Device (PD). Integrating auxiliary power can be a challenging design task and the PoE designer must understand the various methods, inherent tradeoffs, and pitfalls that exist with each method of implementation. The main issues the designer may need to address are power source priority, smooth transitions between different power sources, and inrush current limiting.

Depending on the connection point, there are three basic configurations that are commonly used to add auxiliary power to PoE systems:

- **Option A:** Connection at the front-end of PD (before the pass-FET). It is often called the “Front Aux” technique or “FAUX” option. This is a rarely used option as there is no adapter priority and thus there is wasted power dissipation on the PD chip.
- **Option B:** This is the most commonly used option. Connection at the input of the switching converter of PD (behind the front-end). It is often called the “Rear Aux” technique or “RAUX” option. There is a sub-option that includes an additional high side or low side OR-ing diode. It offers the ability to introduce adapter priority by turning off the pass-FET. There is no wasted power disipation as the current is not flowing through the PD chip.
- **Option C:** Connection at the output voltage of the DC-DC converter of PD. It is called “direct OR-ed” or “output OR-ed”. This option has limited use. It requires the adapter voltage to match output and can not be used with sync rectifiers.

Figure 1. Adding Auxiliary Power



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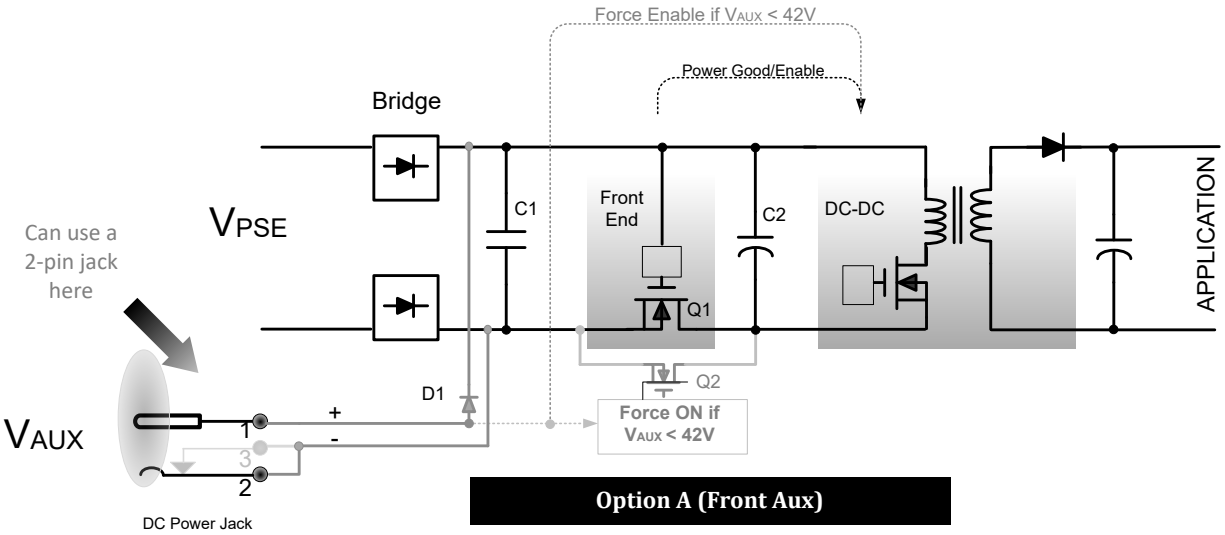
1. Option A (Front Aux or "FAUX" Method)

The main drawbacks of this method are:

- First in, first served
- Impossible to define adapter priority
- Possible current sharing when the PoE and the adapter voltages are close
- PD must support much higher currents

The following figure shows a typical case where the VAUX is within the PoE range.

Figure 1-1. Front Aux Method



If PoE power is present (in other words, voltage VPSE at PD is between 37V and 57V), the VAUX must be greater than the VPSE for the OR-ing diode D1 to conduct (in the following figure). Therefore, "wall-adapter priority" (something that is usually preferred in applications) is not assured. The VAUX takes over only if it is the greater voltage of the two. When that happens, it allows D1 to conduct. If the VAUX is not greater than the VPSE, the application continues to be powered from the PoE rail.

However, if the VPSE is not present initially or it drops out momentarily for whatever reason, then the VAUX allows D1 to conduct. With this configuration, VPSE is injected at the input of the Front End. Therefore, for the application to actually receive power from the AUX rail, the pass-FET (Q1) must conduct. The PD ICs turn ON the pass-FET between 36V to 42V, as per the IEEE® standard, a PD must activate on a rising voltage waveform before it reaches 42V. In other words, if the AUX rail is higher than 42V, the pass-FET turns on and the application then receives power from the AUX rail.

If the VAUX is already providing power while the PSE is switching ON, then it fails to detect the 25 kΩ signature resistor. This is because the VAUX would have charged up the port capacitance in parallel with the 25 kΩ. Therefore, the FAUX method, without the additional provisions, is a case of "first come, first served". If the PSE is providing power, then the AUX rail can take over only if it is greater than the PSE rail, otherwise, the PSE continues to provide power indefinitely. If the AUX rail provides power, then the PSE rail can never come. In this case, only if the AUX rail drops out, the PSE rail can take over.

Note: If the AUX rail is close to the VPSE, it is possible that when D1 conducts, the bridge rectifier may not get fully reverse-biased. Therefore, the PSE may not turn off instantly. Depending on the cable resistance, both the wall-adapter and the PSE may continue to deliver power in some ratio. On closer examination, it is realised that D1 starts to conduct when the VAUX exceeds the port voltage on the PD-side, but for the PSE to stop delivering power completely (bridge rectifier reverse-biased), the VAUX must be equal to or more than the port voltage at the PSE-end. In fact, as per the IEEE standard, the PSE stops delivering power only when the current, it is pushing through, drops below 5 mA. When that happens, it fails to come up again unless the adapter is powered down or unplugged. Summarizing the cases so far (and ignoring diodes forward drops for simplicity):

1. **Larger VAUX:** 42V < VPSE < VAUX (For example, VAUX = 54V, VPSE = 50V). **Wall-adapter priority** (Aux dominance).
   PD application does not get reset if adapter is plugged in. But the PD application resets if adapter is unplugged as PSE is in OFF state.
2. **Smaller VAUX (but in PoE range):** 42V < VAUX < VPSE (For example, VAUX = 48V, VPSE = 54V). **First come, first served.**
   PD application does not get reset if PSE is turned off (provided adapter is already plugged in). However, the PD application resets if the adapter is unplugged.

1.1 Controlling Inrush Currents

Inrush currents during “hot-swap” (change-over from PSE to AUX and vice versa) is a measure issue. In general, there are two voltage sources of unequal voltages. If one takes over (under any conductive condition), a large bulk capacitor can (“C2”, at the input of DC-DC stage) charge up almost immediately, as the pass-FET is on. The inrush current into C2 can be high. Fortunately, OR-ing diodes are rarely damaged when this happens because the diodes typically have a very high non-repetitive surge current ratings. However, any FET in the path of this inrush, such as pass-FET, can be damaged.

The IEEE PoE standard does not demand that the pass-FET Q1 has any active current limitation if C1+ C2 + CPSE is less than 180 µF. To ensure a smooth power-up with Front Aux connection, it is necessary to have not only an inrush current limit, but also an additional operational current limit in the PD if you may need to plug an adapter with voltage greater than VPSE while Q1 is fully conducting. For example, Microchip PD70210 and PD70211 have the operational current limit of about 2.2A. Under normal PoE operation, this default current limit is high enough to remain “transparent”, but under the hot-swap conditions, it enters into the picture to limit inrush and to protect FET. Note that some commercial PD chips rely on thermal shutdown under fault conditions, which is undesirable.

Therefore, it is concluded that to support the Front Aux option, the pass-FET of the front-end must always have a well-defined current limit.

1.2 VAUX Outside PoE Range

So far, the case of VAUX within the normal PoE voltage range is discussed. If VAUX is less than 42V as mentioned, then the PD Front End may not turn on (in other words, the Q1 stops conducting). In theory, this can be overcome by introducing a small boost converter in the adapter line. This wakes up the front-end, which then allows Q1 to conduct.

Another option to support low AUX voltages is to bypass the internal pass-FET (Q1) by an additional external FET (Q2) (see Figure 1-1). Then, the DC-DC stage (in other words, defeat its IEEE-compliant UVLO) needs to be force-enabled. Now, it must be esured not to turn on the external bypass FET (Q2) while still operating (partially or fully) under the PoE power, because that defeats the current limiting function present in Q1. Wait until only D1 is conducting (zero current through the Bridge rectifier), before Q2 is turned on.

To control inrush currents, as Q2 typically has no current limiting (to protect it better from the high inrush currents), it is advisable to insert:

- A small current limiting resistor in series with the OR-ing diode D1
- An NTC (negative temperature coefficient) device in series with the OR-ing diode

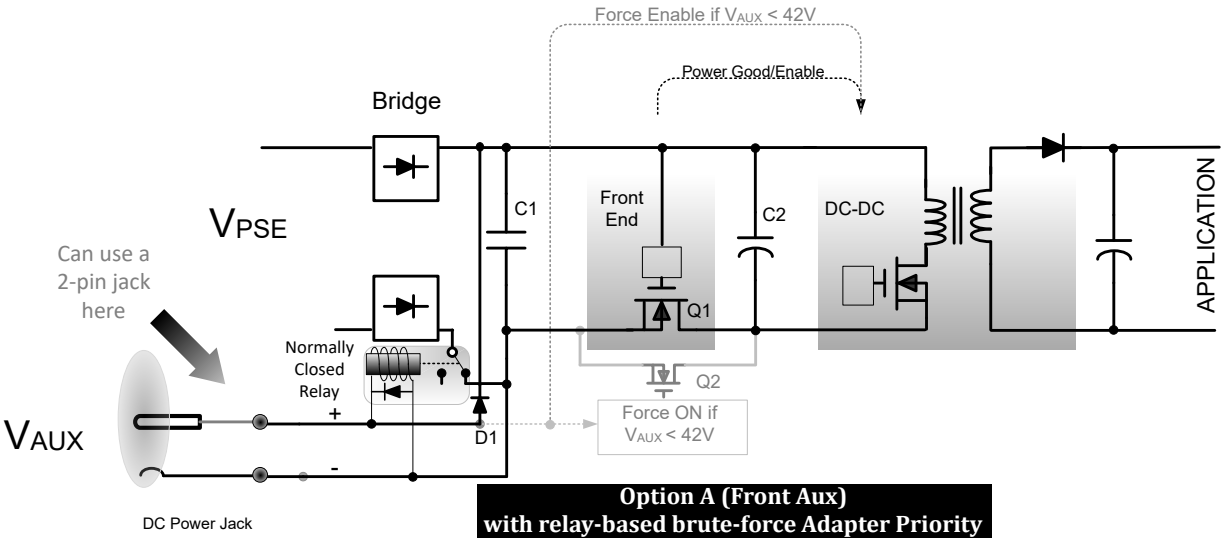
1.3 Brute-Force Wall-Adapter Priority

There is another method to ensure "wall-adapter priority" (Aux dominance) under any condition: by simply disconnecting the PSE power whenever the wall adapter is plugged in. In theory, this could be accomplished by using a three-terminaladapter socket. It is also known as a "2-conductor, interrupting DC power jack".

For this method, the jack current rating should be at least 5A to avoid the contacts from wearing out prematurely and the voltage rating should be well above 60V. Unfortunately, known commercially available multi-terminal jacks are rated only up to 48V and are not intended for interrupting power flow. Their manufacturers state that the power must be turned off before inserting or removing the mating plug. In addition, with such a Configuration, the PSE rail cannot come up until the adapter is not only powered down, but also unplugged from the PD (the male DC plug removed from the jack). Finally, the PD application resets whenever the adapter is plugged into the PD, or when it is unplugged. Because of the above problems, the method with ground switching jack is not practical.

A relay can be used instead of a multi-terminal socket as shown in the following figure. With the relay, a two terminal jack can be used, and the male plug does not have to be manually plugged in or unplugged. Only when there is voltage present on the AUX rail, the relay activates and creates an adapter priority. But once again, if the VAUX is outside the normal PoE operating range, Q1 needs to be forced to conduct (or bypass it with Q2) and the DC-DC converter needs to be force-enabled. However, if more current can not be allowed through Q1 or Q2, the total power is limited significantly if the AUX rail voltage is too low.

Figure 1-2. Front Aux Method (with Relay-Based Brute-Force Adapter Priority)

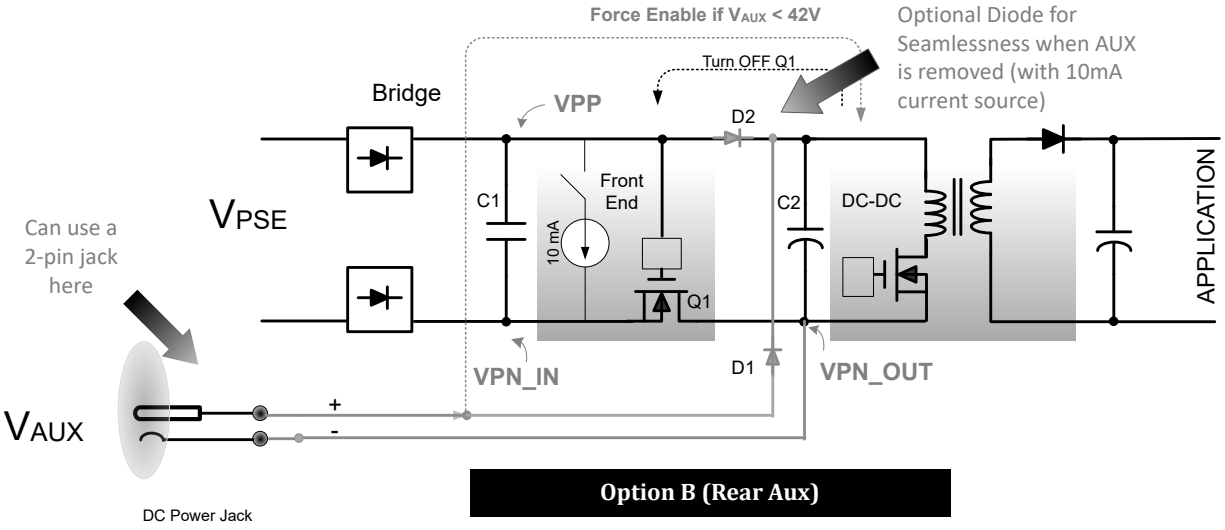


Despite of all the solutions discussed, the Front Aux method is not preferred because an implementation of the Aux power source priority complicates the circuit as the pass-FET of the Front End (Q1) has to be in ON state to deliver power. Instead, the Rear Aux method is a better choice.

2. Rear Aux or “RAUX” Method

This method has the following advantage from a heuristic viewpoint: it introduces the ability to make the PSE to disconnect power if desired by just turning off the pass-FET (“Q1”) of the Front-End. If the PSE current falls below 5 mA, then the PSE typically disconnects, though it is likely to keep attempting detection. The following figure shows the application of Rear Aux.

Figure 2-1. Rear Aux Method



The RAUX method has another major advantage: when the Aux rail is delivering power, its current does not pass through the pass-FET (Q1) of PD and is not limited by the front-end current limit. Therefore, as long as the DC-DC stage can function down to the lower voltages, full power to the application can be provided even for the lower AUX rails.

As in the FAUX method, there are two cases when the AUX rail is within the normal PoE range (ignoring the diode forward drops for simplicity, and assuming that the optional diode D2 is not present so far):

1. **Larger VAUX:** VPSE < VAUX (for example, VAUX = 54V, VPSE = 50V). **Wall-adapter priority** (Aux dominance).
   PD application does not reset if the adapter is plugged in, and it resets when the adapter is unplugged.
2. **Smaller VAUX (but in PoE range):** 42V < VAUX < VPSE (for example, VAUX = 48V, VPSE = 54V). **First come, first served.**

In this case, there is no need for the pass-FET of the Front End (“Q1”) to be in ON state to deliver power.

With RAUX method, there is an ability to forcibly turn off the pass-FET of the front-end when the adapter power is available. Therefore, it is no longer “first come, first served”. This option requires a special pin in the Front End controller. Microchip controllers PD70210A/AL and PD70211 have WA_EN pin that turns off the internal pass FET when the logic High voltage is applied to it. By using this pin, one can enforce the adapter priority regardless of the relation between PoE and adapter voltages. By sensing the voltage on the remote side of the OR-ing diode D1 as per the dashed line marked “RAUX” in Figure 1, one can detect the presence of the AUX rail. Even if VAUX is less than VPSE, by using WA_EN pin, the Aux rail can be forced to dominate for any condition and at all times by simply turning off the pass-FET of the Front End (disconnecting the PSE from the application).

When the pass-FET Q1 is turned off, there are actually two possibilities going forward, the two “sub-options” within this RAUX option as mentioned earlier:

1. **Diode “D2” not present**: The PSE is disconnected and stays disconnected. AS the AUX voltage flows back into the port capacitance (in parallel to the 25 kΩ signature resistor) that prevents the PSE from ever detecting a valid PD and turning on the PoE rail (keeping it in standby, waiting for the AUX rail to be removed). This conserves system power, optimizes power delivery, and allows port power to be allocated to other ports by the host as required. But that “green” feature can also be a disadvantage on resumption of PoE power. Because, the PoE power may not be available immediately if it was meanwhile committed elsewhere. So, though

asserting the adapter priority is seamless (causing no controller’s PD-side reset) when the adapter is either powered down or unplugged, there will be a PD-side reset on resumption of the PoE power.

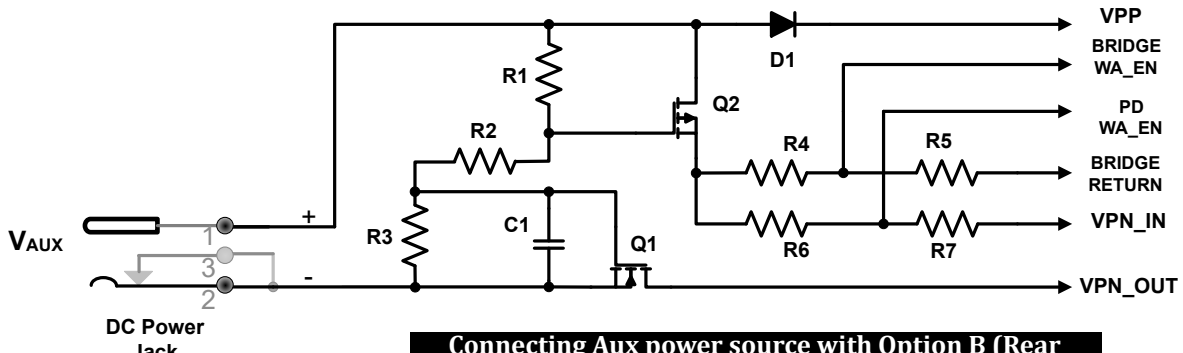
2. **Diode “D2” present**: With this addition, you can choose an option to “keep alive” the PoE rail as a sort-of “UPS standby” if the wall adapters are not delivering power. The diode D2 prevents the negation of the 25 kΩ signature by the AUX rail, so the PSE is able to power up (again). As Q1 is kept in OFF state, the PSE rail does not force its way through D2 based on higher voltage. In other words, Q1 is still in OFF state. But the PSE is not allowed to disconnect after detecting 25 kΩ signature, by keeping the rail alive by drawing a small current to the left of Q1. Therefore, the front-end needs to be designed in such a way that when the wall adapter is sensed through the RAUX pin, the Front End is forced to draw >10 mA from the PSE, preventing MPS disconnect (see the previous figure). In this way, you can have the advantage that if the Aux rail is removed, the PoE rail can seamlessly take over the power delivery (perhaps with the help of some architectural soft-transitioning features). This ensures no interruption in the power and the consequent PD reset.

2.1 Summarizing the RAUX Option

The RAUX option can be summerized as follows:

- Potentially seamless transitioning from the PoE power to the Aux power and back is possible with RAUX, provided the front-end is designed to support this feature with a dedicated WA_EN pin on the front-end. In addition, we need to provide the diode D2 shown in Figure 2-1. Otherwise, the AUX voltage flows back into the port capacitance, in parallel to the 25 kΩ signature resistor, and that prevents the PSE from detecting a valid PD.
- Although, the wall adapter priority is naturally possible if VAUX > VPSE, with the RAUX method, you can easily ensure the unconditional adapter priority with a dedicated WA_EN pin that turns off the pass-FET of the front-end. As with Front Aux, in theory, you can also assure “brute-force” adapter priority by using a relay as shown in the following figure. Unfortunately, all the limitations of the mechanical switch and relay that has been discussed in the Front Aux option, are applicable here too. For one, we are likely going to lose seamlessness under hot-swap conditions.
- Inrush current protection for adapter line is not inherently available with RAUX method, because an adapter is connected after a PD chip. The adapter must protect itself from inrush currents. In addition to this, hot plugging adapter can cause contact arcing in the DC jack. The circuit in the following figure provides “slow start” for the adapter line that limits its surge current and protects contacts from arcing, and enforces adapter priority when used with the Microchip controllers PD70210A/AL and PD70211.

Figure 2-2. Connecting AUX Power Source with Arc Protection and Adapter Priority



The auxiliary FET Q1 limits the initial current from the adapter due to a slow raise of its gate voltage. After the initial WA connection, Q1 is fully turned on and ensures low losses due to its low Rds_on. An additional signal FET Q2 disables the active bridge PD70224 (if used) and the PD controller through dividers R4, R5 and R6, R7.

Recommended values are:

- R1 = 2 kΩ, R2 = 11 kΩ, R3 = 4 kΩ
- C1 = 10 uF/25V
- R4,R6 = 150 kΩ

- R5,R7 = 14.3 kΩ
- Q1-FDS86242
- Q2-ZVP3310FTA

3. Auxiliary Power Option C (Direct OR-ed)

The final option is to connect the Auxiliary power directly to the output of the PD power supply (see Figure 1). The main advantage of this method is the possibility of the seamless transition from adapter power to PoE. As the DC-DC converter is continuing to operate (at no load) even in the presence of DC adapter, its power consumption is usually sufficient to prevent the PSE from turning off. However, this method has a number of disadvantages. In all the previous options, the Aux rail could be unregulated and the PWM/DC-DC stage would carry out the required regulation. This method requires an auxillary power supply designed to deliver the fully regulated voltage required by the PD load. In addition, if the DC-DC converter uses synchronous rectifiers, this configuration also needs an additional OR-ing diode or an FET emulating diode in series with the DC-DC output. This adds cost and leads to additional constant power loss under the regular PoE operation.

4. Conclusion

The preferred method of connecting an auxiliary DC power is the Rear Aux method (Option B) used with the Microchip PD controller that allows turning off an internal pass-FET by a logic “adapter present” signal, such as PD70210A/AL and PD70211.

5. Revision History

Revision	Date	Description
A	April 2020	Initial revision. Previously, the application note in the Microsemi format was referred as TN214.

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